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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/938,686	10/30/2001	Angel Antonio Pepe	IRV1.PAU.53	2551

7590 12/19/2002

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EXAMINER
VU, HUNG K

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/938,686	Applicant(s) PEPE ET AL.	
	Examiner Hung K. Vu	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,13 and 14* is/are rejected.

7)☒ Claim(s) *12,15 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Invention of Group II, Claims 1-16, in Paper No. 7 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Applicant's election without traverse of Invention of Group II, Claims 1-16, in Paper No. 7 is acknowledged.

Claim Objections

2. Claims 1-16 are objected to because of the following informalities:

In claim 1, lines 5-6, between "the integrated" insert --pre-formed--.

In claim 1, lines 7 and 8, "prepared" should be changed to "pre-formed".

In claim 2, line 1, "an interconnect" should be changed to "said interconnect".

In claims 3 and 5, line 1, "an interconnect" should be changed to "said interconnect".

In claim 3, lines 3-4, "opposing sides of said test pad" should be changed to "opposing side of said at least one test pad".

In claim 4, lines 2-3, the phrase "having gold on opposing sides of said test pad and sandwiched therebetween a conductive field metal" should be changed to "having gold on a conductive field metal".

In claim 5, lines 6-7, "opposing sides of said test pad" should be changed to "opposing side of said at least one test pad".

In claim 6, line 2, "a plurality" should be changed to "said plurality".

In claim 6, lines 3-4, the phrase "having gold on opposing sides of said test pad and sandwiched therebetween a conductive field metal" should be changed to "having gold on a conductive field metal".

In claim 7, line 1, "a plurality" should be changed to "said plurality".

In claim 7, line 2, "form" should be changed to "forms".

In claim 8, line 1, "an interconnect" should be changed to "said interconnect".

In claim 8, line 5, "prepared" should be changed to "pre-formed".

In claim 9, lines 2, 3 and 5, "prepared" should be changed to "pre-formed".

In claim 9, line 2, "an integral" should be changed to "said integral".

In claim 10, lines 2 and 4, "prepared" should be changed to "pre-formed".

In claim 10, line 2, "an integral" should be changed to "said integral".

In claim 11, lines 2 and 4, "prepared" should be changed to "pre-formed".

In claim 11, line 2, "an integral" should be changed to "said integral".

In claim 12, line 1, "prepared" should be changed to "pre-formed".

In claim 13, line 1, "the step" should be changed to "a step".

In claim 13, lines 2 and 4(two occurrences), "prepared" should be changed to "pre-formed".

In claim 13, line 2, delete "said".

In claim 13, line 3, between "said test" insert --at least one--.

In claim 14, line 1, "wherein a" should be changed to "further comprising a plurality of interconnect assembly and pre-formed integrated circuit chips wherein said".

In claim 14, line 2, "prepared" should be changed to "pre-formed".

In claim 15, line 1, "wherein a" should be changed to "further comprising a plurality of interconnect assembly and pre-formed integrated circuit chips wherein said".

In claim 15, lines 2 and 5, "prepared" should be changed to "pre-formed".

In claim 16, line 3, "prepared" should be changed to "pre-formed".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-11 and 13-14 are rejected under 35 U.S.C. 102(a) as being anticipated by Kwon et al. (PN 6,235,552).

Kwon et al. discloses, as shown in Figures 19-20 and 26-27, a method of preparing a pre-formed integrated circuit chip for encapsulation in an electronic package comprising the steps of:

forming an interconnect assembly (130) separately from the pre-formed integrated circuit chip (100); (note Figures 6 and 14-15)

forming a plurality of conducive bumps (128) connected to the terminals (104) of the pre-formed integrated circuit chip;

bonding the interconnect assembly to the pre-formed integrated circuit chip; (note Figure 16)

passivating the bonded interconnect assembly and the pre-formed integrated circuit chip into an integral structure to provide the electronic package. (note Figures 17 and 26-27)

With regard to claim 2, Kwon et al. discloses the step of forming the interconnect assembly comprises forming the interconnect assembly on a releasable substrate (110).

With regard to claim 3, Kwon et al. discloses the step of forming the interconnect assembly comprises forming at least one pad (116) in an interconnect layer, which at least one pad can be accessed and electrically connected on opposing side of the pad. Note that the pad is capable to function as a test pad.

With regard to claim 4, Kwon et al. discloses the step of forming at least one test pad forms a test pad having gold on a conductive field metal. (note Col. 3, lines 14-33 and lines 44-48)

With regard to claim 5, Kwon et al. discloses the step of forming the interconnect assembly comprises forming at least one pad (116) in a plurality of stacked interconnect layers, each of which at least one pad in each interconnect layer can be accessed and electrically connected on opposing side of the pad. Note that the pad is capable to function as a test pad.

With regard to claim 6, Kwon et al. discloses the step of forming at least one test pad in the plurality of stacked interconnect layers forms at least one test pad in each layer having gold on a conductive field metal.

With regard to claim 7, Kwon et al. discloses the step of forming the plurality of conductive bumps connected to the terminals of the integrated circuit chip forms a metallic bump making connecting to a terminal o the integrated circuit chip and a solder layer (108) disposed on the metallic bump.

With regard to claim 8, Kwon et al. discloses the step of forming the interconnect assembly comprises forming at least one pad (116) in an interconnect layer, which at least one pad can be accessed and electrically connected on opposing side of the pad, and wherein the step of bonding the interconnect assembly to the pre-formed integrated circuit chip flip bonds the solder layer onto one side of the pad. Note that the pad is capable to function as a test pad.

With regard to claim 9, Kwon et al. discloses the step of passivating the bonded interconnect assembly and the pre-formed integrated circuit chip into the integral structure to provide the electronic package comprises underfilling the pre-formed integrated circuit chip with an insulating material (134,156) to remove all voids between the pre-formed integrated circuit chip and the interconnect assembly.

With regard to claims 10 and 11, Kwon et al. discloses the step of passivating the bonded interconnect assembly and the pre-formed integrated circuit chip into the integral structure to provide the electronic package comprises potting (by layer 156) the interconnect assembly and the pre-formed integrated circuit chip into an integral package.

With regard to claim 13, Kwon et al. discloses the method further comprising a step of accessing the pre-formed integrated circuit chip through electrical connect to at least one pad through a surface thereof opposing the surface of the at least one pad contacting a terminal of the pre-formed integrated circuit chip. Note that the pad is capable to function as a test pad. Also, the pad is capable to use to test the pre-formed integrated circuit chip. (note Figures 18-20, 27 and 31)

With regard to claim 14, Kwon et al. discloses the method further comprising a plurality of interconnect assembly and pre-formed integrated circuit chips wherein the plurality of interconnect assembly and pre-formed integrated circuit chips are bonded together to form a corresponding plurality of electronic packages and further comprising the step of releasing the plurality of electronic packages from each other. (note Figures 20 and 26)

Allowable Subject Matter

4. Claims 12 and 15-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is an examiner's statement of reasons for allowance:

Applicant's claims 12 and 15-16 are allowable over the references of record because none of these references disclose or can be combined to yield the claimed invention such as the method further comprising the step thinning the pre-formed integrated circuit chip, as recited in claim 12, and the method further comprising a plurality of interconnect assembly and pre-formed integrated circuit chips wherein the plurality of interconnect assembly and pre-formed integrated circuit chips are bonded together to form a corresponding plurality of electronic packages and further comprising the step of testing the interconnect assembly and bonding a tested interconnect assembly in the step of bonding the interconnect assembly to the pre-formed integrated circuit chip only if the interconnect assembly tested good, as recited in claim 15.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (703) 308-4079. The examiner can normally be reached on Mon-Thurs 7:00-4:30 and every other Friday 7:00-3:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

December 13, 2002

Hung Vu